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J Bauer, M Bershteyn, I Kaplan, P ... - Proceedings of the 35th ..., 1998 - portal.acm.org
... the transfer of variable information between the processor and the **FPGA** array **...** subcycle timing for the hardware events • It enforces inter-processor lock-step **synchronization**. **...** 7. Limitations Hardware support for event triggers and process **scheduling** increases the performance of **...**
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[PDF] Accelerated logic **simulation** by using prototype boards psu.edu [PDF]
J Haufe, P Schwarz, T Bemdt, J Große - Design, Automation and Test in ..., 1998 - Citeseer
... up, we assume the same simple logical protocol for **simulator** and hardware **synchronization** which is **...** 187-201 [6] J. Willis, Z. Li, ZP Lin: Use of Embedded **Scheduling** to Compile **...** 337-345, Springer Verlag 1996 [24] M. Koch, D. Tavangarian: Einsatz von **FPGA** zur Akzeleration **...**
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The design of RPM: an **FPGA**-based multiprocessor **emulator** psu.edu [PDF]
K Oner, LA Barroso, S Iman, J Jeong, K ... - Proceedings of the ..., 1995 - portal.acm.org
... Extending the **simulation** phase for too long delays the **schedule** while not guaranteeing a correct **...** any board, inter-processor interrupts, software system reset, a backplane hardware barrier **synchronization**, and the **...** D7 D6 D5 D4 D3 D2 D1 D0 CCLK Serial Data per each **FPGA ...**
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[PDF] A survey of hw/sw cosimulation techniques and tools psu.edu [PDF]
H Hübert, A Jantsch - Stockholm, Sweden, Thesis work, Royal Institute of ..., 1998 - Citeseer
... for the target machine, and the HW can be implemented, eg on a **FPGA**, or as an ASIC. Final **...** tion between the system components under **simulation**, and their **synchronization**. Further timing control mechanisms, ensured by **scheduling** policies, are considered. **...**
Cited by 18 - Related articles - View as HTML - All 3 versions

[CITATION] A **simulation** environment for core based embedded systems
F Pétrot, D Hommais, A Greiner - **Simulation** Symposium, 1997 ..., 1997 - ieeexplore.ieee.org
... Emulation of the hardware on a board, using for ex- ample an **FPGA** implementation or an **...** The drawback of this approach reside in the **synchronization** mechanism that needs to communicate from the **...** of the **simulation** time of a sys- tem is spend in the **scheduling** of **simulation ...**
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An approach to mapping the timing behavior of VLSI circuits on **emulators**
PB Sabet, L Vuillemin - rsp, 2001 - computer.org
... communication overhead and the evaluation load [3]. A great emphasis has been specially put on developing different **synchronization** strategies [4 **...** Obviously, the obtained performance must be balanced by the high cost of such distributed **scheduler** in terms of **FPGA** gate **...**
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D Stiliadis, A Varma - IEEE INTERNATIONAL CONFERENCE ON ..., 1996 - Citeseer
... of their inherently serial nature 5]. Communication and **synchronization** bottlenecks also limit the **...** to four cells per cell-time, bu er them, and **schedule** the next cell for transmission. **...** Programming of the **FPGA** devices on the board is accomplished through a programming bus. **...**
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Performance tradeoffs for **emulation**, hardware acceleration, and **simulation**
GD Peterson - System on chip methodologies and design ..., 2001 - books.google.com
... The limited routing available for **FPGAs**, typically results in lower utilization rates of the **...** computations tpAR Time spent on parallel computations tsYNC Time spent on **synchronization** fE Frequency **...** to use each of these verification technologies to best meet the **schedule** and cost **...**
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Instruction set **emulation** for rapid prototyping of SoCs psu.edu [PDF]
J Schnerr, G Haug, W Rosenstiel - ... and Test in Europe-Volume 1, 2003 - portal.acm.org
... These steps include, amongst others, a **scheduling** within blocks and the binding of symbolic **...** For the implementation of these busses the HDL code of the **FPGAs** has to be **...** The **synchronisation** between hardware and the **emulated** software, the handling of bus accesses, and **...**
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